In the Claims:

Claims 1-11 (canceled)

12. (new) An integrated circuit comprising:

A. input pads;

B. output pads;

C. core circuitry coupled between the input pads and the output pads;

D. output circuitry coupled between the core circuitry and the output pads, for each output pad the output circuitry including:

i. a tri-state buffer having a core input lead connected to a core output lead of the core circuitry, a data output lead connected to an output pad and an enable input lead carrying an enable signal that can place the data output of the tri-state buffer in a high impedance state; and

ii. comparator circuitry having a core input lead connected to the core output lead and the core input lead of the tri-state buffer, an encoded response input lead connected to the output pad and the data output lead of the tri-state buffer, and an enable input lead connected to the enable input lead of the tri-state buffer.

13. (new) The integrated circuit of claim 12 in which the comparator circuitry includes a serial scan input lead, a serial scan output lead, a serial scan control input lead and a compare strobe input lead.

14. (new) The integrated circuit of claim 12 in which the encoded response lead carries a trinary signal.

15. (new) The integrated circuit of claim 12 in which the comparator circuitry includes a trinary gate having an input connected to the encoded response input lead, an OR gate

having an input connected to the core input lead, and mask circuitry connected to the outputs of the trinary gate and the OR gate.

16. (new)The integrated circuit of claim 15 in which the enable input lead is coupled to the trinary gate, the OR gate and the mask circuitry.

17. (new)The integrated circuit of claim 12 in which the comparator circuitry includes compare gates, a pass/fail latch, and a scan cell, the compare gates being connected to the core input lead and the encoded response lead, the pass/fail latch being coupled to the output of the compare gates to store the result of a compare, and the scan cell being coupled to the output of the pass/fail latch and having an scan input lead, a scan output lead and a scan control lead.

18. (new)The integrated circuit of claim 17 in which the pass/fail latch includes an AND gate coupled to the compare gates and a flip-flop connected to the AND gate.

19. (new)The integrated circuit of claim 17 in which the scan cell includes a multiplexer connected to the output of the flip-flop, the scan input lead and the scan control lead, and a flip-flop connected to the output of the multiplexer, the scan output lead and the scan control lead.